Society 5.0を支える集積システムの創出

International industry-academic collaboration (CIES consortium) enhances creation of innovative integrated electronic technologies from materials/equipment/devices to LSI/software/system for Society 5.0



東北大学 国際集積エレクトロニクス研究開発センター

Center for Innovative Integrated Electronic Systems (CIES), Tohoku University

- ► Enhancement of global competitiveness in the field of next-generation integrated electronics systems.
- Practical realization of applications of this technology field and creation of new industries.
- Establishment of R&D consortium with industries
- Development of innovative technologies for Integrated systems and creation of new industries.



Tetsuo Endoh **Director of CIES**







Power Electronics

MTJ/CMOS hybrid technology

Brain computing Neuromorphic computing

GaN on Si technology



1st Science Park

campus

300mm process line &

evaluation tools in TU's







Higher energy efficiency for automotive and industrial

Technologies





- frame work
- World-class IPs and its strategic management
- Global standard join research contract

Variety of core technologies & deep understanding under "Research First" principle

Innovative Technologies for Energy-Saving & Intelligence

Spintronics

- CMOS/spintronics fusion technologies
- ●3D-structured silicon device technologies
- ●loT edge computing device technologies, etc.

Al Hardware

- Brain-type nonvolatile IC technologies
- Intelligent computing system technologies, etc.

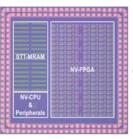
Power Electronics

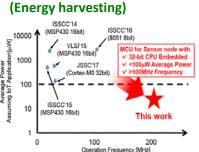
- GaN/Si power device technologies
- Low-loss hybrid power integrated device technologies
- High-efficiency power electronics technologies
- ●Innovative power management system technologies, etc.

World-Leading Accomplishments

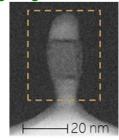
STT-MRAM based AI processor (12 cores)

Ultralow power FPGA MCU @47µW





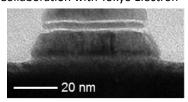
Single-digit-nanometer MJT



MMM 2016 JJAP 2016 SEMICON China 2017

Reactive etching process suitable for high-density STT-MRAM manufacturing

Collaboration with Tokyo Electron



Tohoku Univ. Press Release May 2018

ISSCC 2019 Measurement system

Collaboration with **Keysight Technologies**

for STT-MRAM

Tohoku Univ. Press Release September 2017 & May 2018

Nature Communication 2018 Memory LSI tester for STT-MRAM

Collaboration with Advantest, TOKYO SEIMITSU, MICRONICS JAPAN, Toei Scientific

Industrial

