東北大学 電気通信研究所

研究室外部評価資料

(2013 年度-2018 年度)

Activity Report of Research Laboratory for External Review

April 2013 - March 2019
(FY.2013-2018)

Research Institute of Electrical Communication

Tohoku University

新概念 VLSI システム研究室

New Paradigm VLSI System

A. 研究室名 / Research Laboratory

新概念 VLSI システム研究室 / New Paradigm VLSI System

B. 構成員 / Faculty and Research Staff (as of May 1, 2019)

※ 欄を適宜追加削除等調整して下さい．期間内に異動等があった場合には，在籍期間を記載して下さい．

教授 / Professor	
氏名 /Name	羽生　貴弘 / Takahiro Hanyu (April 2002-)
分野名 / Research Field	新概念 VLSI システム研究分野 / New Paradigm VLSI System
准教授 / Associate Professor	
氏名 / Name	夏井 雅典 / Masanori Natsui (April 2008 -)
分野名 / Research Field	新概念 VLSI デザイン研究分野 / New Paradigm VLSI Design
助教 / Assistant Professor	
氏名 / Name	鬼沢 直哉 / Naoya Onizawa (Dec. 2013 -) (FRIS*所属(Dec.2013-Oct.2018)) (FRIS*所属：鈴木 大輔 / Daisuke Suzuki (April 2015 -)) *東北大学学際科学ﾌﾛﾝﾃｨｱ研究所
他 / Others	
	産学官連携研究員: 1 名/Posdoc fellow (Oct. 2009 – Mar. 2014) 産学官連携研究員: 1 名/Posdoc fellow (Oct. 2009 – Mar. 2015) 産学官連携研究員: 1 名/Posdoc fellow (Nov. 2012 – Jun. 2016) 産学官連携研究員: 1 名/Posdoc fellow (Apr. 2013 – Mar. 2014) 産学官連携研究員: 1 名/Posdoc fellow (Oct. 2013 – Nov. 2013) 産学官連携研究員: 1 名/Researcher (Apr. 2015 -)

C. 研究目的 / Research Purpose

超大規模半導体集積回路（Very Large Scale Integration; VLSI）チップ，およびそれを応用した VLSI システムは，電子機器の「頭脳」として機能しており，現代社会のあらゆる産業製品や社会基盤の質を決定している．VLSI システムの高度化・高性能化・高信頼化は，今日に至るまで，主に材料・デバイスの極限微細加工技術により推進されてきた．しかし，この微細化技術一辺倒による性能向上は，いずれ限界に達すると予想されている．本研究室では，従来までのシリコン CMOS 回路方式のみでなく，新しい材料・新デバイス特性を積極的に活用した「新概念」の回路設計・実現方式およびシステムアーキテクチャについて研究し，従来技術の延長による VLSI システムの限界を打破することを研究目的とする．

Rapid progress in recent deep submicron regime has led the capability to realize giga-scaled embedded systems on a chip (SoC), while performance degradation of SoCs due to wiring complexity, power dissipation and device-characteristic variation are increasingly getting serious problems in the recent Very Large Scale Integration (VLSI) chip. Our research activity is to solve the above problems primarily by the following two ways: the logic-in-memory architecture based on nonvolatile logic, and the brainware LSI (BLSI) computing, which would open up a novel VLSI chip paradigm, called a “new-paradigm VLSI system.”

D. 主な研究テーマ / Research Topics

1. 不揮発性 logic-in-memory architecture とその超低電力 VLSI システムに関する研究
2. デバイスモデルベース新概念コンピューティングアーキテクチャに関する研究
3. ポストバイナリ情報表現・非同期式制御に基づく高性能 NoC に関する研究
4. 確率的演算に基づく低消費電力 LSI 設計技術に関する研究

1. Nonvolatile logic-in-memory VLSI architecture and its application to ultra-low-power VLSI processors and systems
2. Device-model-based new-paradigm VLSI computing architecture
3. Asynchronous-control/post-binary data coding-based circuit for a high-performance NoC (Network-on-Chip)
4. Low-power LSI design technology based on stochastic logic / probabilistic computation

E. 学術論文等の編数 / The Number of Research Papers

	2013	2014	2015	2016	2017	2018	Total
(1) 査読付学術論文 Refereed journal papers	14	15	6	8	9	7	59
(2) 原著論文と同等に扱う 査読付国際会議発表論文 Full papers in refereed conference proceedings equivalent to journal papers	2	2	1	1	0	1	7
(3) 査読付国際会議 Papers in refereed conference proceedings	12	17	12	12	8	6	67
(4) 査読なし国際会議・シンポジウム等 Papers in conference proceedings	4	3	2	3	4	3	19
(5) 総説・解説 Review articles	0	0	0	0	2	0	2
(6) 査読付国内会議 Refereed proceedings in domestic conferences	0	0	0	0	0	0	0
(7) 査読なし国内研究会・講演会 Proceedings in domestic conferences	11	12	11	9	16	7	66
(8) 著書 Books	0	1	1	1	0	2	5
(9) 特許 Patents	24	3	4	10	7	4	52
(10) 招待講演 Invited Talks	2	5	3	6	9	10	35

F. 特筆すべき研究成果 / Significant Research Achievements (FY.2013-2018)

See Ref. 1. "#" mark indicates research carried out at a former organization.

2013-2018 年度の研究成果（論文・特許など）のうち，前半（2013-2015 年度）と後半（2016-2018 年度）それぞれで代表的な数件（2-3 件程度ずつ）について，参考資料を引用して，その特徴と学術的意義などを簡単に紹介する．英文のみ，もしくは和文と英文で記載．
要約は 300 字程度．論文誌の要約/Abstract のコピー可．学術面での国際的インパクトならびに社会的影響を 100 字程度で記載．
必ずしも当該期間内に発表・出版したものに限るのではなく，例えば過去に発表したものでもこの期間内に成果が得られたり，評価されるようになったりしたものも含むものとする．
インパクトファクターや被引用件数など，できる限り第三者が定量的に評価できる指標を用いてアピールすること．それらの指標にはそぐわない場合には，その事情とそれに変わる適当な評価指標・尺度を示すこと．

[2013-2015]

1. N. Sakimura, Y. Tsuji, R. Nebashi, H. Honjo, A. Morioka, K. Ishihara, K. Kinoshita, S. Fukami, S. Miura, N. Kasai, T. Endoh, H. Ohno, T. Hanyu, and T. Sugibayashi, "A 90nm 20MHz Fully Nonvolatile Microcontroller for Standby-Power-Critical Applications," 2014 IEEE ISSCC, Dig. Tech. Papers, pp.184-185, Feb. 2014. [Times Cited: 68]

Abstract:

Recently there has been increased demand for not only ultra-low power, but also high performance, even in standby-power-critical applications. Sensor nodes, for example, need a microcontroller unit (MCU) that has the ability to process signals and compress data immediately. A previously reported 130nm CMOS and FeRAM-based MCU features zero-standby power and fast wakeup operation by incorporating FeRAM devices into logic circuits [1]. The 8MHz speed, however, was not sufficiently high to meet application requirements, and the FeRAM process also has drawbacks: low compatibility with standard CMOS, and write endurance limitations. A spintronics-based nonvolatile integrated circuit is a promising option to achieve zero standby power and high-speed operation, along with compatibility with CMOS processes. In this work, we demonstrate a fully nonvolatile 16b MCU using 90nm standard CMOS and three-terminal SpinRAM technology. It achieves 20MHz, 145μW/MHz operation with a 1V supply in the active state, and 4.5μW intermittent operation with 120ns wakeup time and 0.1% active ratio, without forwarding of re-boot code from memory. The features provide sufficiently long battery life to achieve maintenance-free sensor nodes.

International impact on both academic and social aspects:

We have newly developed a microcontroller circuit (hereinafter MCU: Micro Control Unit) for wireless sensor terminals applying spintronics logic integrated circuit technology, and in its operation experiments, compared to the conventional technology, the power consumption of the MCU is up to 1/80. This extends the battery life of the sensor terminal equipped with the MCU to approximately 10 times. It is an international conference presentation paper that applies this technology to a microcontroller unit for IoT sensor nodes, has been adopted by ISSCC, the world's top international conference in the field, and has a cited reference of 68.

2. M. Natsui, D. Suzuki, N. Sakimura, R. Nebashi, Y. Tsuji, A. Morioka, T. Sugibayashi, S. Miura, H. Honjo, K. Kinoshita, S. Ikeda, T. Endoh, H. Ohno, and T. Hanyu, "Nonvolatile Logic-in-Memory LSI Using Cycle-Based Power Gating and its Application to Motion-Vector Prediction," IEEE Journal of Solid-State Circuits (JSSC), vol. 50, no. 2, pp. 476-489, Feb. 2015. [IF: 5.173], [Times Cited: 32]

Abstract:

A magnetic tunnel junction (MTJ)-based logic-in-memory hardware accelerator LSI with cycle-based power gating is fabricated using a 90 nm MTJ/MOS process on a 300 mm wafer fabrication line for practical-scale, fully parallel

motion-vector prediction, without wasted power dissipation. The proposed nonvolatile LSI is designed by establishing an automated design environment with MTJ-based logic-circuit IPs and peripheral assistant tools, as well as a precise MTJ device model produced by the fabricated test chips. Through the measurement results of the fabricated LSI, this study shows both the impact of the power-gating technique in a fine temporal granularity utilizing the non-volatility of the MTJ device and the effectiveness of the established automated design environment for designing random logic LSI using nonvolatile logic-in-memory.

International impact on both academic and social aspects:

JSSC is the most prestigious journal on solid-state circuit, which clearly indicates the extremely-high impact of this paper to the related research area. The potential capability of nonvolatile logic-in-memory LSI has been confirmed through the fabrication and measurement, however, large-scale logic integrated circuits usually have a large number of MTJ devices that are arranged in a complex and irregular manner, requiring the use of automatic design tools that can be applied to a nonvolatile logic-in-memory circuit. This paper presents the developed design flow including primitive cell library and circuit simulator for nonvolatile logic-in-memory LSI, and also demonstrates the world-first fabricated nonvolatile logic-in-memory chip using automated design flow.

[2016-2018]

1. M. Natsui, D. Suzuki, A. Tamakoshi, T. Watanabe, H. Honjo, H. Koike, T. Nasuno, Y. Ma, T. Tanigawa, Y. Noguchi, M. Yasuhira, H. Sato, S. Ikeda, H. Ohno, T. Endoh, and T. Hanyu, "An FPGA-Accelerated Fully Nonvolatile Microcontroller Unit for Sensor-Node Applications in 40nm CMOS/MTJHybrid Technology Achieving 47.14μW Operation at 200MHz," 2019 IEEE International Solid-State Circuits Conference (ISSCC2019), pp.202-203, February 2019. [Times Cited: 0]

Abstract:

Recently, the demand for low-power, high-performance microcontroller units (MCUs) for power-supply-critical sensor node applications has been increasing. In response to this demand, the use of nonvolatile memory elements for realizing MCUs for sensor node applications has been actively researched and developed. The latest nonvolatile MCUs (NV-MCUs) demonstrated 32b operation at 30MHz and 8b operation at 100MHz. However, this performance level is not suitable for sensor node applications that process large numbers of received signals and extract valuable information from them immediately to reduce the amount of transfer data to a data center. The use of various nonvolatile devices has also been proposed. However, these devices exhibit critical drawbacks when applied to sensor node applications, including limited endurance and low compatibility with standard CMOS. A spintronics-based nonvolatile device with unlimited endurance, a short switching time, and CMOS compatibility is a promising candidate for designing a low-power, high-performance NV-MCU.

International impact on both academic and social aspects:

It is an international conference presentation paper that applies the technology to a microcontroller unit for IoT sensor nodes, and is adopted by ISSCC, the world's top international conference in the field, and is also selected as one of the highlight papers in the conference. Related to this achievement, the 5th CIES Technology Forum / DAY 1 International Symposium gave an invited talk on the theme of “Impact of MTJ-Based Nonvolatile Microcontroller LSI for IoT Applications” and also took only two months after the publication of this achievement. There were already two invited talks and one talk request.

2. A. Ardakani, F. Leduc-Primeau, N. Onizawa, T. Hanyu, and W. J. Gross, “VLSI Implementation of Deep Neural

Networks Using Integral Stochastic Computing," IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 25, no. 10, pp. 2688-2699, Oct. 2017. [IF: 1.946], [Times Cited: 76]

Abstract:

The hardware implementation of deep neural networks (DNNs) has recently received tremendous attention: many applications in fact require high-speed operations that suit a hardware implementation. However, numerous elements and complex interconnections are usually required, leading to a large area occupation and copious power consumption. Stochastic computing (SC) has shown promising results for low-power area-efficient hardware implementations, even though existing stochastic algorithms require long streams that cause long latencies. In this paper, we propose an integer form of stochastic computation and introduce some elementary circuits. We then propose an efficient implementation of a DNN based on integral SC. The proposed architecture has been implemented on a Virtex7 field-programmable gate array, resulting in 45% and 62% average reductions in area and latency compared with the best reported architecture in the literature. We also synthesize the circuits in a 65-nm CMOS technology, and we show that the proposed integral stochastic architecture results in up to 21% reduction in energy consumption compared with the binary radix implementation at the same misclassification rate. Due to fault-tolerant nature of stochastic architectures, we also consider a quasi-synchronous implementation that yields 33% reduction in energy consumption with respect to the binary radix implementation without any compromise on performance.

International impact on both academic and social aspects:

In this research, energy saving of brain type LSI that imitates brain function is performed by utilizing stochastic operation which is a kind of stochastic operation. As a brain-type LSI, deep learning and auditory filter were realized by stochastic calculation, and as a result, significant power reduction was achieved. It achieves significant power reduction compared to the conventional method by using stochastic operation for hardware realization of deep neural networks, which has been accepted to IEEE TLVSI and has already been cited in 76 cases.

3. T. Hanyu, T. Endoh, D. Suzuki, H. Koike, Y. Ma, N. Onizawa, M. Natsui, S. Ikeda, and H. Ohno, "Standby-Power-Free Integrated Circuits Using MTJ-Based VLSI Computing," in *Proceedings of the IEEE*, vol. 104, no. 10, pp. 1844-1863, Oct. 2016. [IF: 10.694], [Times Cited: 36]

Abstract:

Nonvolatile spintronic devices have potential advantages, such as fast read/write and high endurance together with back-end-of-the-line compatibility, which offers the possibility of constructing not only stand-alone RAMs and embedded RAMs that can be used in conventional VLSI circuits and systems but also standby-power-free high-performance nonvolatile CMOS logic employing logic-in-memory architecture. The advantages of employing spintronic devices, especially magnetic tunnel junction (MTJ) devices with CMOS circuits, are discussed, and the current status of the MTJ-based VLSI computing paradigm is presented along with its prospects and remaining challenges.

International impact on both academic and social aspects:

This paper was accepted for the journal (Proceeding of IEEE) with the highest impact factor of 10.964 in this research field. We have studied MTJ-based nonvolatile logic circuits for the decade and summarized the recent results. This research has been recently extended to design low-energy brainware LSI using CMOS/MTJ devices. As a result, the basic research (S) has been accepted.

G. 特筆すべき活動 / Significant Activities (FY.2013-2018)

See Ref. 2-9. "#" mark indicates research carried out at a former organization.

研究室外部評価参考資料の 2 以降を参照しながら，2013-2018 年度のなどの活動の中から特筆すべきものを取り出し，前半（2013-2015 年度）と後半（2016-2018 年度）に分けて簡単に紹介する．英文のみ，もしくは和文と英文で記載.

[2013-2015]

1. IEEE Computer Society Technical Committee of Multiple-Valued Logic, Chair（Jan. 2014 – Dec. 2015

Election of the next "two-year (2014-2015) chairperson" at IEEE Computer Society Technical Committee of Multiple-Valued Logic (TC-MVL) was held at the end of 2013. Dr. Takahiro Hanyu was elected as the chairperson of the above IEEE Computer Society TC-MVL, because he had been contributed as program chairpersons, local arrangement chairpersons at the international symposium on multiple-valued logic (ISMVL). It is the third successive generation to have been appointed as chairperson from Asia/Pacific region at ISMVL held since 1971. At that time, the number of submitted and accepted manuscripts from the Asian/Pacific region was not very high, but from this period the number of manuscripts submitted and accepted from the Asian/Pacific region has increased, and this trend continues to the present.

2. Estimated requirements "Brain-type LSI creation business for realization of human judgment" (Apr. 2014 – Mar. 2020)

The research activities have been spreading in a local newspaper "Kahoku Shinpo", academic article (Han. 30, 27) "One step to realize brain-type computer", "Nikkei Sangyo Shimbun" (June, 2015) about the research introduction about "brain type LSI" project newly started from H 26 April May 5) "The brain type computer · development third honest?", and Nihon Keizai Shimbun (September 27, 2015) "Circuit to judge like brain". In addition, contact points with the international researcher community are being established through the brain-type LSI-related international symposium, and we have made efforts to make a good start out of the research project promotion concerned.

3. Minister of Education, Culture, Sports, Science and Technology Minister's Award for Science and Technology Award (Research Division) (Apr. 15, 2015)

With regard to "non-volatile logic in-memory integrated circuit" technology promoted by this research team, we gave an opportunity to widely recognize the usefulness and future prospects at overseas famous international conferences, such (1) an invited talk at the world's top international conference on electronic device technology, IEDM (held in Dec. 2014), (2) an Invited lecture at FORUM of the world's top international conference on technology, ISSCC 2015 (held in Feb. 2015), and (3) an invited talk in Europe's largest and highest international conference on VLSI design technology DATE '15 (held in March 2015). Based on such recognition from the researcher community, the Minister of Education, Culture, Sports, Science and Technology receives an award from the Ministry of Education, Culture, Sports, Science and Technology Award for research on nonvolatile logic in-memory integrated circuits. The "non-volatile logic" related technology, which has been promoted since 2002, has been recognized in Japan and overseas.

[2016-2018]

1. 2016 IEEE International Symposium on Multiple-Valued Logic, Symposium Chair (June 2015 – May 2016)

   Multiple-valued logic research is a society (about 100 people) with approximately half of mathematicians, so the annual expenses can not be worked out by the participation expenses alone, and the participation expenses have been held in the past two years (Germany, Canada) I had to make it abnormally high ($ 840 for IEEE member, $ 1,000 for non-member). On the other hand, at the 2016 Japan Conference (Chairman: Hanyu), he made efforts to acquire external funds (including application and adoption to various foundations including NICT), reduced registration to about half, and facilitated participation . As a result, we got a large number of participants (about 1.2 times the average year) and were able to hand over money to IEEE. This payment was used as a “Subsidy from IEEE” at the ISMVL meeting (2018) held two years later, and therefore contributed significantly to the holding of this international conference.

2. Grant-in-Aid for Scientific Research (S) (FY 2016 – 2020) (127,000,000 JPY)

   We will open the possibility to realize brain-type computing by focusing on asynchronous control that is intrinsically used in brain information processing and applying a dark silicon approach to it, where an asynchronous circuit structure is suitable for power gating function and its operation principle, and practical brain. These researches were developed as a joint research project (H26 / B09: Brain-type LSI international joint research, representative: Takahiro Hanyu), and promoted as a research fund, Grant-in-Aid for Scientific research (S) (FY 2016 - 2020) in addition to being accepted by IEEE TETC (IF: 3.826), which is the highest academic journal, as well as being adopted exclusively by the Japanese at ASYNC 2017, the highest international conference in asynchronous circuits and systems, a total of five cases have been received at international conferences. It is highly regarded in the field, such as giving an invited lecture.