SSDM Paper Award

Studies on Static Noise Margin and Scalability for Low-Power and High-Density Nonvolatile SRAM using Spin-Transfer-Torque (STT) MTJs

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Takashi Ohsawa was born in Tokyo on Feb. 16, 1954. He received BS and MS degrees in physics from Waseda University, Tokyo, Japan in 1977 and 1979, respectively, and Ph.D. in electronic engineering from University of Tsukuba, Tsukuba, Japan in 2009. He worked for Toshiba mainly on DRAM development for 28 years from 1982 to 2010. He developed four generations from 1Mb, 4Mb, 64Mb and to 256Mb DRAMs. From 1997 to 2000, he participated in the DRAM Development Alliance with IBM and then Siemens as a design manager in Vermont, USA. From 2000 to 2007, he initiated 1T-DRAM development in Toshiba that was called floating body cell (FBC) as an alternative to the 1T-1C DRAM that is facing scaling issues. Since 2010, he has been a professor in Center for Spintronics Integrated Systems, Tohoku University, Sendai, Japan.

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